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Problem Set 1
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# Verification

## Problem 1: VIS and Verilog warm-up [2 Points]

In the following exercises we are going to use the hardware verification tool VIS. Install the latest version of VIS (`http://vlsi.colorado.edu/~vis/`) or use the Virtual Machine provided on the course website. Consider the following Verilog program (also available on the course website):

```
module x (a, b, c);
  input a;
  input b;
  output c;
  wire a;
  wire b;
  reg [2:0] c;

  initial begin
    c = 0;
  end

  always @(posedge a) begin
    if (b)
      c = c + 3;
    else
      c = c;
  end
endmodule
```

1. Describe what the progam does. [1 Point]
2. Give an example output for a simulation run with 5 steps. [1 Point]

## Problem 2: Counters [3 Points]

1. Write the Verilog description of an 2-Bit Counter with an additional `reset` flag. Whenever the `reset` flag is set, the next configuration must output $\langle 00\rangle_2$. [1 Point]
2. Write the Verilog description of an 8-Bit Counter:
   a) Using four 2-Bit Counter as submodules [1 Point]
   b) Without using submodules [1 Point]

The following exercises belong to the afternoon session.

## Problem 3: CTL warm-up [3 Points]

Express the following properties as CTL formulas over $AP = \{a, b, c\}$ and provide a justification. For more complicated formulas, also comment on their subformulas!

1. There exists a path on which the following holds for every state $s$: there exists a path which starts in $s$, and on which eventually $a$ holds and in the next state, $\neg a$ holds. [1 Point]

2. There exists a reachable state $s$ for which the following holds: $a$ is true and on all paths starting from $s$, $c$ holds as long as $b$ does not hold. [1 Point]

3. On every path the following holds for every state: $a$ is valid if and only if $b$ is valid and in the previous state, $c$ is valid. [1 Point]

## Problem 4: CTL Semantics [4 Points]

Prove or disprove the following implications:

1. Let $\Phi_1 = \mathsf{AF}\, a \vee \mathsf{AF}\, b$ and $\Phi_2 = \mathsf{AF}\,(a \vee b)$.
   Prove or disprove $\Phi_1 \rightarrow \Phi_2$ and $\Phi_2 \rightarrow \Phi_1$. [2 Points]

2. Now consider $\Psi_1 = \mathsf{E}\,(a \,\mathsf{U}\, \mathsf{E}\,(b \,\mathsf{U}\, c))$ and $\Psi_2 = \mathsf{E}\,(\mathsf{E}\,(a \,\mathsf{U}\, b) \,\mathsf{U}\, c)$.
   Again, prove or disprove $\Psi_1 \rightarrow \Psi_2$ and $\Psi_2 \rightarrow \Psi_1$. [2 Points]