Verification

Lecture 18

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REVIEW: Timed automaton semantics

The transition relation \rightarrow is defined by the following two rules:

- Discrete transition: $\langle \ell, v \rangle \xrightarrow{d} \langle \ell', v' \rangle$ if all following conditions hold:
 - there is an edge labeled $(g : \alpha, D)$ from location ℓ to ℓ' such that:
 - g is satisfied by v, i.e., $v \models g$
 - v' = v with all clocks in *D* reset to 0, i.e., v' = reset D in v
 - v' fulfills the invariant of location ℓ' , i.e., $v' \models inv(\ell')$
- **Delay** transition: $\langle \ell, v \rangle \xrightarrow{\alpha} \langle \ell, v+d \rangle$ for positive real d
 - if for any $0 \le d' \le d$ the invariant of ℓ holds for v+d', i.e. $v+d' \models inv(\ell)$

REVIEW: Timelock, time-divergence and Zenoness

 A timed automaton is only considered an adequate model of a time-critical system if it is:

non-Zeno and timelock-free

 Time-convergent paths will be explicitly excluded from the analysis.

REVIEW: Timed CTL

Syntax of TCTL <u>state-formulas</u> over AP and set C:

$$\Phi ::= \mathsf{true} \left| \begin{array}{c} a \end{array} \right| \left| \begin{array}{c} g \end{array} \right| \left| \begin{array}{c} \Phi \end{array} \wedge \left| \begin{array}{c} \Phi \end{array} \right| \left| \begin{array}{c} \neg \Phi \end{array} \right| \left| \begin{array}{c} \mathsf{E} \varphi \end{array} \right| \left| \begin{array}{c} \mathsf{A} \varphi \end{array} \right|$$

where $a \in AP$, $g \in ACC(C)$ and φ is a path-formula defined by:

$$\varphi ::= \Phi U^{J} \Phi$$

where $J \subseteq \mathbb{R}_{\geq 0}$ is an interval whose bounds are naturals Forms of J: [n, m], (n, m], [n, m) or (n, m) for $n, m \in \mathbb{N}$ and $n \leq m$

for right-open intervals, $m = \infty$ is also allowed

REVIEW: Semantics of TCTL

For state $s = \langle \ell, \eta \rangle$ in *TS*(*TA*) the satisfaction relation \vDash is defined by:

s ⊨ true		
$s \vDash a$	iff	$a \in L(\ell)$
$s \vDash g$	iff	$\eta \vDash g$
$S\vDash \neg \Phi$	iff	not $s \models \Phi$
$\mathbf{S} \vDash \Phi \ \land \ \Psi$	iff	$(s \models \Phi)$ and $(s \models \Psi)$
$s \vDash E \varphi$	iff	$\pi \vDash \varphi$ for some $\pi \in Paths_{div}(s)$
$s \vDash A \varphi$	iff	$\pi \vDash \varphi$ for all $\pi \in Paths_{div}(s)$

path quantification over time-divergent paths only

REVIEW: TCTL model checking

• TCTL model-checking problem: $TA \models \Phi$ for non-Zeno TA

$TA \vDash \Phi$	iff	$TS(TA) \vDash \Phi$
\smile		
timed automaton		infinite state graph

- Idea: consider a finite region graph RG(TA)
- Transform TCTL formula Φ into an "equivalent" CTL-formula $\widehat{\Phi}$
- Then: $TA \vDash_{\mathsf{TCTL}} \Phi$ iff $RG(TA) \vDash_{\mathsf{CTL}} \widehat{\Phi}$

finite state graph

REVIEW: Eliminating timing parameters

- Eliminate all intervals $J \neq [0, \infty)$ from TCTL formulas
 - introduce a fresh clock, z say, that does not occur in TA
 - $s \models E \diamondsuit^{J} \Phi$ iff reset z in $s \models \diamondsuit(z \in J \land \Phi)$
- Formally: for any state s of TS(TA) it holds:

$$s \vDash \mathsf{E} \Phi \mathsf{U}^{\mathsf{J}} \Psi \quad \text{iff} \quad \underbrace{\mathsf{s}\{z := \mathsf{0}\}}_{\text{state in } \mathsf{TS}(\mathsf{TA} \oplus z)} \vDash \mathsf{E} \mathsf{E} \left((\Phi \lor \Psi) \mathsf{U} (z \in \mathsf{J}) \land \Psi \right)$$

$$s \vDash A \Phi U^{J} \Psi$$
 iff $\underbrace{s\{z := 0\}}_{\text{state in TS(TA \oplus z)}} \vDash A ((\Phi \lor \Psi) U (z \in J) \land \Psi)$

• where $TA \oplus z$ is TA (over C) extended with $z \notin C$

REVIEW: Clock equivalence

Impose an equivalence, denoted \cong , on the clock valuations such that:

(A) Equivalent clock valuations satisfy the same clock constraints g in *TA* and Φ :

$$\eta \cong \eta' \Rightarrow \begin{pmatrix} \eta \vDash g & \text{iff} & \eta' \vDash g \end{pmatrix}$$

- no diagonal clock constraints are considered
- all the constraints in TA and Φ are thus either of the form x ≤ c or x < c</p>
- (B) Time-divergent paths emanating from equivalent states are equivalent
 - this property guarantees that equivalent states satisfy the same path formulas
- (C) The number of equivalence classes under \cong is finite

REVIEW: First observation

- $\eta \models x < c$ whenever $\eta(x) < c$, or equivalently, $\lfloor \eta(x) \rfloor < c$
 - ▶ $\lfloor d \rfloor = \max \{ c \in \mathbb{N} \mid c \leq d \}$ and $frac(d) = d \lfloor d \rfloor$
- $\eta \models x \le c$ whenever $\lfloor \eta(x) \rfloor < c$ or $\lfloor \eta(x) \rfloor = c$ and $frac(\eta(x)) = 0$
- ⇒ $\eta \models g$ only depends on $\lfloor \eta(x) \rfloor$, and whether $frac(\eta(x)) = 0$
 - Initial suggestion: clock valuations η and η' are equivalent if:

 $\lfloor \eta(x) \rfloor = \lfloor \eta'(x) \rfloor$ and $frac(\eta(x)) = 0$ iff $frac(\eta'(x)) = 0$

▶ Note: it is crucial that in *x* < *c* and *x* ≤ *c*, *c* is a natural

REVIEW: Second observation

- Consider location l with inv(l) = true and only outgoing transitions:
 - one guarded with $x \ge 2$ (action α) and y > 1 (action β)
- Let state $s = \langle \ell, \eta \rangle$ with $1 < \eta(x) < 2$ and $0 < \eta(y) < 1$
 - α and β are disabled, only time may elapse
- ► Transition that is enabled next depends on x < y or x ≥ y</p>
 - e.g., if $frac(\eta(x)) \ge frac(\eta(y))$, action α is enabled first
- Suggestion for strengthening of initial proposal for all x, y ∈ C by:

 $frac(\eta(x)) \leq frac(\eta(y))$ if and only if $frac(\eta'(x)) \leq frac(\eta'(y))$

REVIEW: Final observation

- So far, clock equivalence yield a denumerable though not finite quotient
- For $TA \models \Phi$ only the clock constraints in TA and Φ are relevant
 - let $c_x \in \mathbb{N}$ the <u>largest constant</u> with which x is compared in TA or Φ
- \Rightarrow If $\eta(x) > c_x$ then the actual value of x is irrelevant
 - ► constraints on \cong so far are only relevant for clock values of x(y) up to $c_x(c_y)$

Clock equivalence

Clock valuations η , $\eta' \in Eval(C)$ are <u>equivalent</u>, denoted $\eta \cong \eta'$, if:

(1) for any
$$x \in C$$
: $(\eta(x) > c_x) \land (\eta'(x) > c_x)$ or
 $(\eta(x) \le c_x) \land (\eta'(x) \le c_x)$

(2) for any $x \in C$: if $\eta(x), \eta'(x) \leq c_x$ then:

 $\lfloor \eta(x) \rfloor = \lfloor \eta'(x) \rfloor$ and $frac(\eta(x)) = 0$ iff $frac(\eta_2(x)) = 0$

(3) for any $x, y \in C$: if $\eta(x), \eta'(x) \le c_x$ and $\eta(y), \eta'(y) \le c_y$, then:

 $\operatorname{frac}(\eta(x)) \leq \operatorname{frac}(\eta(y))$ iff $\operatorname{frac}(\eta'(x)) \leq \operatorname{frac}(\eta'(y))$.

$$s \cong s'$$
 iff $\ell = \ell'$ and $\eta \cong \eta'$

Clock equivalence is a bisimulation

Clock equivalence is a bisimulation equivalence over AP'

Regions

• The clock region of $\eta \in Eval(C)$, denoted $[\eta]$, is defined by:

$$[\eta] = \{ \eta' \in Eval(C) \mid \eta \cong \eta' \}$$

• The state region of $s = \langle \ell, \eta \rangle \in TS(TA)$ is defined by:

$$[s] = \langle \ell, [\eta] \rangle = \{ \langle s, \eta' \rangle \mid \eta' \in [\eta] \}$$

Number of regions

The number of clock regions is bounded from below and above by:

$$|C|! * \prod_{x \in C} c_x \leq | \underbrace{Eval(C)/\cong}_{\text{number of regions}} | \leq |C|! * 2^{|C|-1} * \prod_{x \in C} (2c_x + 2)$$

where for the upper bound it is assumed that $c_x \ge 1$ for any $x \in C$

the number of state regions is |Loc| times larger

Preservation of atomic properties

1. For $\eta, \eta' \in Eval(C)$ such that $\eta \cong \eta'$:

 $\eta \vDash g$ if and only if $\eta' \vDash g$ for any $g \in AP' \smallsetminus AP$

2. For $s, s' \in TS(TA)$ such that $s \cong s'$:

 $s \models a$ if and only if $s' \models a$ for any $a \in AP'$

where AP' includes all atomic propositions and atomic clock constraints in TA and Φ .

Unbounded and successor regions

- ► Clock region $r_{\infty} = \{ \eta \in Eval(C) \mid \forall x \in C. \eta(x) > c_x \}$ is unbounded
- r' is the successor (clock) region of r, denoted r' = succ(r), if either:

1.
$$r = r_{\infty}$$
 and $r = r'$, or

2.
$$r \neq r_{\infty}, r \neq r'$$
 and $\forall \eta \in r$:

 $\exists d \in \mathbb{R}_{>0}. \ (\eta + d \in r' \quad \text{and} \quad \forall 0 \le d' \le d, \eta + d' \in r \cup r')$

• The successor region: $succ(\langle \ell, r \rangle) = \langle \ell, succ(r) \rangle$

Region automaton

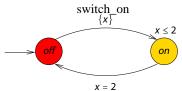
For non-Zeno *TA* with $TS(TA) = (S, Act, \rightarrow, I, AP, L)$ let:

$$RG(TA, \Phi) = (S', Act \cup \{\tau\}, \rightarrow', I, AP', L') \text{ with}$$

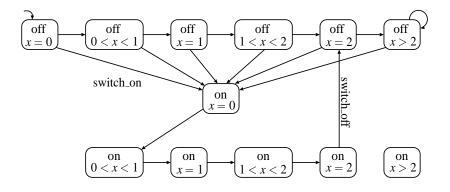
S' = S/ ≅ = { [s] | s ∈ S } and I' = { [s] | s ∈ I }, the state regions
L'(⟨ℓ, r⟩) = L(ℓ) ∪ { g ∈ AP' \ AP | r ⊨ g }
→' is defined by:
$$\frac{ℓ \stackrel{g:\alpha,D}{\rightsquigarrow} ℓ' \quad r ⊨ g \quad reset D in r ⊨ inv(ℓ')}{⟨ℓ, r⟩ \stackrel{\alpha}{\longrightarrow} ' ⟨ℓ', reset D in r⟩} \quad and$$

$$\frac{r ⊨ inv(ℓ) \quad succ(r) ⊨ inv(ℓ)}{⟨ℓ, r⟩ \stackrel{\tau}{\longrightarrow} ' ⟨ℓ, succ(r)⟩}$$

Example: simple light switch



switch_off



Time convergence

For non-Zeno *TA* and $\pi = s_0 s_1 s_2 \dots$ an initial, infinite path in *TS*(*TA*): (a) π is <u>time-convergent</u> $\Rightarrow \exists$ state region $\langle \ell, r \rangle$ such that for some *j*:

 $s_i \in \langle \ell, r \rangle$ for all $i \ge j$

(b) If \exists state region $\langle \ell, r \rangle$ with $r \neq r_{\infty}$ and an index *j* such that:

 $s_i \in \langle \ell, r \rangle$ for all $i \ge j$

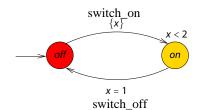
then π is time-convergent

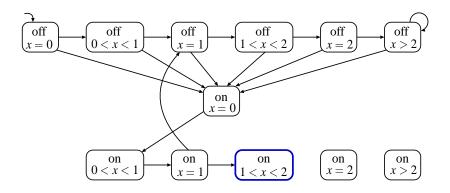
Timelock freedom

For non-Zeno TA:

TA is timelock-free iff no reachable state in RG(TA) is terminal

Example





Correctness theorem

Let TA be a non-Zeno timed automaton and Φ a $\mathsf{TCTL}_{\diamondsuit}$ formula. Then:

$$\underbrace{TA \models \Phi}_{\text{TCTL semantics}} \quad \text{iff} \quad \underbrace{RG(TA, \Phi) \models \Phi}_{\text{CTL semantics}}$$

Overview TCTL model checking

Require: timed automaton *TA* and TCTL formula Φ (both over *AP* and *C*) **Ensure:** *TA* $\models \Phi$

 $\widehat{\Phi} :=$ eliminate the timing parameters from Φ ;

determine the equivalence classes under \cong ;

construct the region graph TS = RG(TA);

apply the CTL model-checking algorithm to check $TS \models \widehat{\Phi}$;

 $TA \models \Phi$ if and only if $TS \models \widehat{\Phi}$

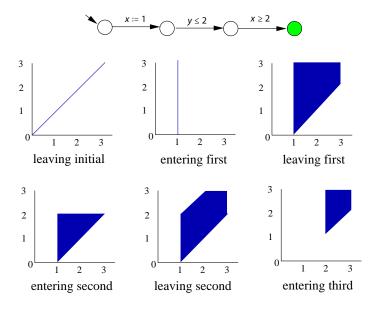
Other verification problems

- 1. The TCTL model-checking problem is PSPACE-complete
- 2. The model-checking problem for timed LTL (and TCTL*) is undecidable

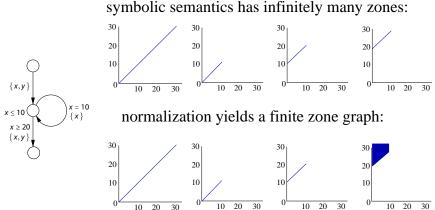
Zones

- Clock constraints are <u>conjunctions</u> of atomic constraints
 - x < c and x y < c for $< \in \{<, \le, =, \ge, >\}$
 - restrict to TA with <u>only conjunctive clock constraints</u>
 - and (as before) assume no difference clock constraints
- A <u>clock zone</u> is the set of clock valuations that satisfy a clock constraint
 - a clock zone for g is the maximal set of clock valuations satisfying g
- Clock zone of g: [[g]] = { $\eta \in Eval(C) \mid \eta \models g$ }
 - ▶ use *z*, *z*′ and so on to range over zones
- The state zone of $s = \langle \ell, \eta \rangle \in TS(TA)$ is $\langle \ell, z \rangle$ with $\eta \in z$

Zone automaton: intuition



Normalization: intuition



symbolic semantics has infinitely many zones:

Successor and reset zones

► z' is the successor (clock) zone of z, denoted $z' = z^{\uparrow}$, if:

$$\flat z^{\uparrow} = \{ \eta + d \mid \eta \in z, d \in \mathbb{R}_{>0} \}$$

- z' is the zone obtained from z by resetting clocks D:
 - reset D in $z = \{ reset D$ in $\eta \mid \eta \in z \}$

Zone graph

For non-Zeno TA let:

$$ZG(TA, \Phi) = (Q, Q_0, E, L')$$
 with

- $Q = Loc \times Zone(C)$ and $Q_0 = \{ \langle \ell, z_0 \rangle \mid \ell \in Loc_0 \}$
- $L(\langle \ell, z \rangle) = L(\ell) \cup \{g \mid g \in z\}$
- *E* consists of two types of edges:
 - Discrete transitions: $\langle \ell, z \rangle \xrightarrow{\alpha} \langle \ell', \text{reset } D \text{ in } (z \land g) \land inv(\ell') \rangle$ if $\ell \xrightarrow{g:\alpha,D} \ell'$, and
 - Delay transitions: $\langle \ell, z \rangle \xrightarrow{\tau} \langle \ell, z^{\uparrow} \land inv(\ell) \rangle$.

Correctness (1)

For timed automaton *TA* and any initial state $\langle \ell, \eta_0 \rangle$:

Soundness:

$$\underbrace{\langle \ell, \underbrace{\{\eta_0\}}_{z_0} \rangle \to^* \langle \ell', z' \rangle}_{\text{in } ZG(TA)} \quad \text{implies} \quad \underbrace{\langle \ell, \eta_0 \rangle \to^* \langle \ell', \eta' \rangle}_{\text{in } TS(TA)} \text{ for all } \eta' \in z'$$

Completeness:

$$\underbrace{\langle \ell, \eta_0 \rangle \to^* \langle \ell', \eta' \rangle}_{\text{in } TS(TA)} \text{ implies } \underbrace{\langle \ell, \{ \eta_0 \} \rangle \to^* \langle \ell', z' \rangle}_{\text{in } ZG(TA)} \text{ for some } z' \text{ with } \eta' \in z'$$

Zone normalization

- To obtain a finite representation, <u>zone normalization</u> is employed
- For zone *z*, $norm(z) = \{ \eta \mid \eta \cong \eta', \eta' \in z \}$
 - where \cong is the clock equivalence
- There can only be finitely many normalized zones
- $\langle \ell, z \rangle \rightarrow_{norm} \langle \ell', norm(z') \rangle$ if $\langle \ell, z \rangle \rightarrow \langle \ell', z' \rangle$

Correctness (2)

For timed automaton *TA* and any initial state $\langle \ell, \eta \rangle$:

Soundness:

$$\langle \ell, \{\eta_0\} \rangle \rightarrow_{\textit{norm}}^* \langle \ell', z' \rangle$$
 implies $\langle \ell, \eta_0 \rangle \rightarrow^* \langle \ell', \eta' \rangle$

- for all $\eta' \in z'$ such that $\forall x. \eta'(x) \leq c_x$
- Completeness:

 $\langle \ell, \eta_0 \rangle \rightarrow^* \langle \ell', \eta' \rangle$ with $\forall x. \eta'(x) \le c_x$ implies $\langle \ell, \{\eta_0\} \rangle \rightarrow^*_{norm} \langle \ell', z' \rangle$

- for some z' such that $\eta' \in z'$
- Finiteness: the transition relation \rightarrow_{norm} is finite

Forward reachability algorithm

Passed := \emptyset : // explored states so far Wait := { (ℓ_0, z_0) }; // states to be explored while Wait $\neq \emptyset$ // still states to go **do** select and remove (ℓ, z) from Wait; if $(\ell = \text{goal} \land z \cap z_{\text{goal}} \neq \emptyset)$ then return "reachable"! fi; if $\neg(\exists (\ell, z') \in \mathsf{Passed}, z \subseteq z') // \mathsf{no}$ "super"state explored yet **then** add (ℓ, z) to Passed // (ℓ, z) is a new state foreach (ℓ', z') with $(\ell, z) \rightarrow_{norm} (\ell', z')$ **do** add (ℓ', z') to Wait; // add symbolic successors fi od

return "not reachable"!