## Embedded Systems 2010/2011 - Assignment Sheet 8

Due: Tuesday, $18^{\text {th }}$ January 2011, before the lecture (i.e., 10:10)
Please indicate your name, matr. number, email address, and which tutorial you are planning to attend on your submission. We encourage you to collaborate in groups of up to three students. Only one submission per group is necessary. However, in the tutorials every group member must be capable to present each solution.

## Exercise 1: A/D Conversion

During the lecture we presented the successive approximations method as one possibility for converting analog signals into digital values. Using the successive approximations method, carry out the conversion of the input voltages $U_{\text {in }}=2.8 \mathrm{~V}, 1.6 \mathrm{~V}$, and 3.55 V into the corresponding binary values. In each case, and for each step of the conversion, show:
(a) the arranged comparison voltage $U_{r e f}$;
(b) the binary value after each comparison.

The digital value should have a precision of 4 bits. Assume also that the working range of the A/D converter lies between $U_{\min }=1 V\left(0000_{2}\right)$ and $U_{\max }=4 V\left(1111_{2}\right)$.

## Exercise 2: Instruction Set Architecture

For each of the following subtasks, decide whether the described differences between the processor variants should be reflected in the instruction set architecture (thereby being visible to software). Justify your answers by brief explanations. Assume that the processors are identical except for the specific difference stated in each subtask.
(a) Processor $A$ uses hardwired control while processor $B$ uses microcode control.
(b) Processor $A$ is a RISC machine while processor $B$ is a CISC machine.
(c) The pipeline of processor $A$ has more stages than the pipeline of processor $B$, but both have full bypassing.

## Exercise 3: Processor Performance

Assume that we split some stage of a pipeline of a processor into two substages. For each of the following subtasks, decide whether the statement is true or false. Justify your answers by brief explanations.
(a) The instructions per program decrease.
(b) The cycles per instruction decrease.
(c) The seconds per cycle decrease.

